UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/623,243 | 07/17/2003 | Ashish D. Alawani | 0140111 | 2882 |

25700 7590 05/30/2006

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

| EXAMINER | |
|---|---|
| LEVI, DAMEON E | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2841 | |

DATE MAILED: 05/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/623,243 | ALAWANI ET AL. | |
| | Examiner | Art Unit | |
| | Dameon E. Levi | 2841 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04/03/2006(Appeal Brief)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3-7,9-16 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,9-16 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *N/A* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

## REOPENED PROSECUTION

Applicant's arguments in the Appeal Brief, filed 04/03/2006, with respect to the rejection(s) of claim(s) 1, 3-7, 9-16, and 18-20 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the prior art below. Prosecution on the merits of this application is reopened.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

**Claims 1, 3-7, 9-16, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al US Patent 6521997**

**Regarding claim** 1, Huang et al discloses a module comprising:

a surface mount component(elements 15,15' Figs 1-4) situated over a laminate circuit board(elements 10,1' Figs 1-4) the surface mount component comprising a first terminal(elements 150 Figs 1-4) and a second terminal(elements 151 Figs 1-4);

a first and a second pad situated on the laminate circuit board, (elements 12, Figs 1-4) the first pad being connected to the first terminal and the second pad being connected to the second terminal(elements 12,150,151, Figs 1-4),

a solder mask trench (elements 13, Figs 1-4) situated underneath the surface mount component, wherein the solder mask trench is situated over a top surface of the laminate circuit board, wherein a solder mask (elements 11, Figs 1-4) uniformly covers said top surface of said laminate circuit board, and wherein said solder mask does not cover said solder mask trench(elements 11,13, Figs 1-4),

wherein a bottom surface of the surface mount component and the top surface of the laminate circuit board form a moldable gap (elements 152, 16, Figs 1-4) the moldable gap including the solder mask trench(elements 13,16 Figs 1-4), wherein the moldable gap and the solder mask trench facilitate a flow of a molding compound underneath the surface mount component, and wherein the solder mask trench is filled with the molding compound (see column 3, lines 37-50).

**Regarding claim** 3, Huang et al discloses wherein the moldable gap is filled with the molding compound(see column 3, lines 37-50).

**Regarding claim** 4, Huang et al discloses further comprising an overmold(elements 17 Figs 1-4), the overmold being situated over the surface mount component.

**Regarding claim** 5, Huang et al discloses wherein the surface mount component is selected from the group consisting of a resistor, a capacitor, an inductor, a diplexer, a diode, and a SAW filter ( elements 15, Figs 1-4)

**Regarding claim** 6, Huang et al discloses wherein the moldable gap has a height of between approximately 45.0 micrometers and 65.0 micrometers ( elements 16, Figs 1-4).

**Regarding claim** 7, Huang et al discloses wherein the overmolded module is an MCM (Figs 1-4).

**Regarding claim** 9, Huang et al discloses a module comprising:

a surface mount component(elements 15,15' Figs 1-4) situated over a laminate circuit board(elements 10,1', Figs 1-4), the surface mount component comprising a first terminal and a second terminal(elements 151,152 Figs 1-4); a first and a second pad situated on the laminate circuit board(elements 15, Figs 1-4) , the first pad being connected to the first terminal and the second pad being connected to the second terminal, (elements 151,152,12 Figs 1-4);

a moldable gap(elements 16, Figs 1-4) situated underneath the surface mount component, the moldable gap comprising a solder mask trench (elements 13, Figs 1-4), wherein the solder mask trench is situated over a top surface of the laminate circuit board (elements 11, 10, Figs 1-3), wherein a solder mask (elements 11, Figs 1-4)uniformly covers said top surface of said laminate circuit board, and wherein said solder mask does not cover said solder mask trench(elements 11,13, Figs 1-4), wherein the moldable gap and the solder mask trench facilitate a flow of a molding compound

underneath the surface mount component, and wherein the solder mask trench is filled with the molding compound (see column 3, lines 37-50)

**Regarding claim** 10, Huang et al discloses wherein the moldable gap is filled with the molding compound(see column 3, lines 37-50).

**Regarding claim** 11, Huang et al discloses further comprising an overmold(elements 17, Figs 1-4), the overmold being situated over the surface mount component.

**Regarding claim** 12, Huang et al discloses wherein the overmold comprises the molding compound (elements 17, Figs 1-4 ,column 3, lines 37-50).

**Regarding claim** 13,Huang et al discloses wherein the moldable gap has a height of between approximately 45.0 micrometers and 65.0 micrometers(elements 16, Figs 1-4)

**Regarding claim** 14, Huang et al discloses wherein the surface mount component is selected from the group consisting of a resistor, a capacitor, an inductor, a diplexer, a diode, and a SAW filter (elements 15, Figs 1-4).

**Regarding claim** 15, Huang et al discloses wherein the overmolded module is an MCM(Figs 1-4,).

**Regarding claim** 16, Huang et al discloses a module comprising:

a surface mount device(elements 15, Figs 1-4) situated over a laminate circuit board(elements 10,1', Figs 1-4), the surface mount device comprising a plurality of terminals(elements 151,152, Figs 1-4);a plurality of pads situated on the laminate circuit board(elements 12, Figs 1-4), each of the plurality of pads being connected to a respective one of the plurality of terminals(elements 151,152,12, Figs 1-4);

a solder mask trench(elements 13, Figs 1-4) situated underneath the surface mount device, wherein the solder mask trench is situated over a top surface of the laminate circuit board(elements 13, 10, Figs 1-4), wherein the moldable gap and the solder mask trench facilitate a flow of a molding compound underneath the surface mount component(elements 34,26,32 Figs 1-3) , and wherein a solder mask (elements 11, Figs 1-4)uniformly covers said top surface of said laminate circuit board, and wherein said solder mask does not cover said solder mask trench(elements 13, 11, Figs 1-4) wherein the solder mask trench is filled with the molding compound (column 3, lines 37-50).

**Regarding claim** 18, Huang et al discloses wherein the surface mount device is a leadless surface mount device ( elements 15, Figs 1-4).

**Regarding claim** 19, Huang et al discloses wherein the surface mount device comprises at least one component, the at least one component being selected from the group consisting of an active component and a passive component ( elements 15, Figs 1-4).

**Regarding claim** 20, Huang et al discloses wherein the overmolded module is an MCM( elements 15, Figs 1-4).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dameon E. Levi whose telephone number is (571) 272-2105. The examiner can normally be reached on Mon.-Fri. (9:00 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dameon E Levi
Examiner
Art Unit 2841

DEL

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800